

PROGRAMMABLE LOCK DETECTOR AND CORRECTOR**ABSTRACT OF THE DISCLOSURE**

An apparatus and method for programmable lock detection and correction (PLDC) to a programmable accuracy in a digital delay-locked loop (DLL) based multiphase clock generator (MCG) is based on a DLL that utilizes a digital count to control the delay of a digitally controlled, multiple-tap delay line in its feedback path where stability of the digital count is used to qualify the determination of lock to a programmable accuracy and lock determination is based on combinatorial evaluation of the multiple phase outputs for the proper waveform relationships. The incidence of false lock corresponding to excessive delay through the delay line is addressed by a LOOPRESET signal that results in a reset of the digital count that controls the delay through the delay line. Additionally, programmability of the stability interval, the digital counter step size, and the accuracy of the lock provide control over lock acquisition time.